REMARKS

In view of the above amendments and the following remarks, reconsideration is requested.

As required, the Title of the invention has been changed to "Video Signal Processor and Video Signal Processing Method which Interpolate a Video Signal Using an Interpolation Factor Based on Phase Information of a Selected Clock."

The Specification has been reviewed and revised to correct minor errors. No new matter has been added.

Figure 9 has been labeled "Prior Art" as suggested by the Examiner.

Claims 1-5 were rejected under 35 U.S.C. § 102(b) as being anticipated by Yoneno. This rejection is traversed and is believed to be inapplicable to claims 1-5 as amended for the following reasons.

Phase Information of Selected Clock Converted Into an Interpolation Factor

Each of claims 1-5 includes recitations directed to:

(1) selection of a clock that is most synchronized with a reference signal from among the plural clocks outputted by respective plural delay elements;

(2) outputting phase information of the selected clock;

(3) converting the phase information into an interpolation factor; and

(4) interpolating the video data signal read from the memory using the interpolation factor.

Thus, according to the inventions recited in claims 1-5, one of the clocks output from the delay elements is selected, and phase information of the selected clock is converted into an interpolation factor by which the video data signal is interpolated.

As an example of such features, please refer to Figs. 1-3, and page 16, line 5 to page 19, line 14 of the present application. According to this example, the clocks S104-S107 are shifted in phase with each other by 1/4 clock. This phase information would correspond to interpolation factors for clocks S104-S107 as 1/4, ½, 3/4, and 1, respectively, once converted to an interpolation factor. Among the clocks S104-S107, the clock S106 is the most synchronized with reference signal S103. Therefore, clock S106 is selected. The phase information of clock S106 is converted into an

interpolation factor S109 of 3/4. In this example, the video data signal S110 read from the memory is interpolated according to S111 = (S110-S201) * S109 + S201. See specifically Figs. 2 and 3.

As recognized by the Examiner, the Yoneno reference discloses that a clock is selected from among plural clocks output by delay elements, respectively (see Fig. 3 and column 11, lines 41-44), and that there is some type of interpolation performed (see column 18, line 64 to column 19, line 12). However, Yoneno does not disclose or in any way suggest outputting phase information of the selected clock, converting the phase information into an interpolation factor, and interpolating the video data signal read from the memory using the interpolation factor as recited in claims 1-5. In the system of Yoneno, there is no relationship between the interpolation and any phase information of the selected clock. The only mention by Yoneno of any phase information with respect to the interpolation is that the phase deviation in the line of memory being processed can be neglected. See column 18, lines 59-60. Accordingly, it is clear that Yoneno does not disclose converting phase information of the selected clock into an interpolation factor. Therefore, claims 1-5 are not anticipated by Yoneno.

Delayed Clocks Are for Generating Interpolation Factor, Not as a Clock for Reading From Memory

The fundamental difference between the claimed invention and the system of Yoneno can be readily seen by comparing Fig. 1 (or Fig. 7) of the present invention with Fig. 1 (or Fig. 12) of Yoneno. Thus, as recited in claims 1, 2, and 5, the video data signal is written to the memory according to a first clock, and the video data signal is read from the memory according to a second clock. The second clock is delayed by plural delay elements, a clock is selected therefrom and, based thereon, an interpolation factor is determined as discussed in detail above. However, as recited in claims 1, 2, and 5, it is the second clock that is the clock for reading the video data signal from the memory, not any of the delayed clocks from the delay elements. Similarly, claims 3 and 4 recite that both the reading and writing are done according to the first clock, that the first clock is delayed by plural delay elements, a clock is selected therefrom and, based thereon, an interpolation factor is determined as discussed in detail above. However, as recited in claims 3 and 4, it is the first clock that is the clock for reading the video data signal from the memory, not any of the delayed clocks

from the delay elements.

The inventions recited in claims 1-5 are in complete contrast with the system of Yoneno. As shown in Figs. 1 and 12 of Yoneno, the input clock 102 is delayed by the delay 10, and the selected output of the delay 201 is the clock for reading the memory 4. This arrangement is shown in the Prior Art Fig. 8 of the present application. The problems associated with an arrangement such as that shown in Prior Art Fig. 8 (and Figs. 1 and 12 of Yoneno) are discussed in detail in the present specification, e.g., one of the periods of the clock becomes a length which is outside of a specified range. The present invention as recited in claims 1-5 solve these problems by converting the phase information of the selected clock into an interpolation factor by which the video data signal read from the memory is interpolated. Yoneno does not disclose or in any way suggest such an arrangement. Accordingly, claims 1-5 are not anticipated by Yoneno.

In view of the above, it is submitted that the present application is in condition for allowance. The Examiner is invited to contact the undersigned by telephone to resolve any remaining issues.

Respectfully submitted,

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